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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/044,087 | 01/09/2002 | Bryan K. Casper | 42390P11940 | 7565 |
| 8791 | 7590 | 05/18/2005 | EXAMINER | |
| BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR LOS ANGELES, CA 90025-1030 | | | JOSEPH, JAISON | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2634 | |

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/044,087

Applicant(s)

CASPER ET AL.

Examiner

Jaison Joseph

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 5, 12 and 17 is/are rejected.
- 7) ☐ Claim(s) 3, 4, 6 - 11, 13 - 16, and 18 - 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION***Priority***

This application is indicated a foreign priority on an application filed in Japan (2001 – 13786) on January 22, 2001. Applicant has not acknowledged the filing of any foreign application in the Oath and declaration and the Office has not received a certified copy of foreign application. In order to claim the priority, applicant is required to submit a new Oath and Declaration and certified copy of the foreign priority.

Double Patenting

Claims 1 and 2 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 or claim 25 of U.S. Patent No. 6,621,323. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 on the patent recite a method of a driver driving data symbols into a transmission line while simultaneously driving plurality of nodes to another node, determining a difference between a signal level from the transmission line and a signal level from the other node and applying the difference to a signal input of a variable offset comparator. The claim 1 or claim 25 does not recite applying plurality of binary values to an offset control input of the comparator, to adjust the viable reference level prior to the comparator performing the comparison. However it is inherent that the reference values must loaded prior performing comparison. Otherwise there are no values to compare.

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Regarding claim 2, which inherits the limitations of claim 1, further the claim 1 or claim 25 in the patent recite sampling a signal from the transmission line and the signal from the other node prior to determining the difference.

Claims 5 and 17 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 or claim 19 of U.S. Patent No. 6,621,323. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 8 recite a circuit comprising a first driver having an output to be coupled to transmission line, a second driver being coupled to receive the same sequence of outgoing data symbols, a subtraction circuit having a first input to be coupled to the transmission line and a second input to the output of the second driver, a comparator having an input coupled to an output of subtraction circuit, the comparator having a substantially variable offset that is controllable to represent a variable reference level; an output of comparator to provide a value that represents a comparison between a signal level at the comparator input and the variable reference level, a control level, and a control circuit having an output that is coupled to an offset control input of the comparator. The claim 6 or claim 19 does not recite the control circuit is to provide a first binary value that corrects for one of a mismatch between the first and second drivers and a mismatch in the subtraction circuit. However, it is inherent that a controller circuit is needed for generating a control signal.

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Regarding claim 12, claimed apparatus including the features corresponding to subject matter mentioned above in rejection of claim 5 is applicable hereto.

Claim 12 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 6 or claim 19 of U.S.

Patent No. 6,621,323 in view of Rostoker et al (US Patent 5,715,274).

Regarding claim 12, claimed apparatus including the features corresponding to subject matter mentioned above in rejection of claim 5 is applicable hereto. The claim 6 or 19 failed to mention a printed wiring board on a parallel bus is formed, an integrated circuit chip package being operatively installed on the board to communicate using the parallel bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the bus. However Rostoker et al teach a printed wiring board on a parallel bus is formed, an integrated circuit chip package being operatively installed on the board to communicate using the parallel bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the bus (see column 6, line 58 – column 7, line 5). Therefore it would be obvious to an ordinary skilled in the art at the time the invention was made to implement a digital serial interface having a low power requirement in an integrated circuit (see column 3, lines 3 – 4).

Allowable Subject Matter

Claims 3, 4, 6 – 11, 13 – 16, and 18 – 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jaison Joseph whose telephone number is (571) 272-6041. The examiner can normally be reached on M-F 8:30 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Jaison Joseph

05/05/05

A handwritten signature in black ink, appearing to read 'Shin', with a long horizontal line extending to the right.

**STEPHEN CHIN
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER 2600**